METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL

ABSTRACT OF THE DISCLOSURE

A phase splitter is formed by first and second branches that generate respective first and second complimentary output clock signals from an input clock signal. The first branch includes two series connected inverters, the first of which receives the input clock signal and the second of which outputs a non-complimentary output clock signal. The second branch includes three series connected inverters, the first of which receives the input clock signal and the third of which outputs a complimentary output clock signal. An inverter is coupled from the output of the second inverter in the second branch to the output of the first inverter in the first branch to increase the slew rate of the signal applied to the input of the second inverter. In one embodiment, first and second parallel pairs of diode-coupled transistors are coupled from the output of the third inverter in the second branch to the outputs of respective first inverters in the first and second branches. In another embodiment, the second branch includes five series connected inverters, and the first and second pairs of diode-coupled transistors are coupled from the outputs of the third and fifth inverters, respectively, in the second branch. These diode-coupled transistors compensate for process variations in the transistors used in the inverters in each branch.